

WHAT IS CLAIMED IS:

1. A reset circuit which includes a plurality of modules from a first stage to a last stage for executing desired functions, and initializes each of the plurality of modules arranged in a semiconductor integrated circuit,
5 comprising:

input means for inputting a reset signal to initialize the plurality of modules; and

pulse generation means connected to the input means to generate a reset pulse based on the reset signal,
10 wherein:

the plurality of modules include a first module arranged at a first stage which is connected to an output of the pulse generation means and receives the reset pulse to be initialized, and a second module arranged at a next
15 stage;

the first module has first control means for generating a first reset signal to initialize the second module, and outputting the first reset signal to the second
20 module after initialization in the first module; and

the second module has second control means which is connected to an output of the first module, receives the first reset signal output from the first module to be initialized, generates a second reset signal to initialize
25 a module arranged at a further next stage based on the first reset signal from the first module, and outputs the second reset signal after initialization in the second

module.

2. The reset circuit according to claim 1,
wherein the first module includes a first register
5 initialized in response to the reset pulse, and the second
module includes a second register initialized in response
to the first reset signal.

3. The reset circuit according to claim 1,
10 wherein the pulse generation means generates the reset
pulse of a pulse width corresponding to predetermined delay
time of the reset signal input to the input means.

4. The reset circuit according to claim 1,
15 wherein the first control means includes:
first detection means which receives a plurality
of initialization notices from the first module to detect
an end of the initialization therein; and
means for generating the first reset signal based
20 on a detection result of the first detection means.

5. The reset circuit according to claim 1,
wherein the second control means includes:
second detection means which receives a plurality
25 of initialization notices from the second module to detect
an end of the initialization therein; and
means for generating the second reset signal based

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on a detection result of the second detection means.

6. A reset circuit which includes a plurality of modules, and initializes each of the plurality of modules arranged in a semiconductor integrated circuit, comprising:

reset input means for inputting a reset signal to initialize the plurality of modules;

clock input means for inputting a clock signal;

control means connected to the reset input means to output, upon detection of the reset signal, a control signal corresponding to the reset signal for a period until a last delayed reset signal is input for a module of a last stage; and a plurality of delay means connected to the clock input means to delay an input signal in synchronization with the clock signal, and to output a delayed reset signal generated by the delaying, wherein:

the plurality of modules are connected corresponding to the plurality of delay means, operated in synchronization with the clock signal, and initialized in synchronization with the clock signal based on the control signal and the delayed reset signal; and

among the plurality of delay means, first delay means arranged at a first stage receives the control signal of the control means as the input signal, and each of second delay means arranged at stages thereafter receives the delayed reset signal output from delay means arranged at a previous stage as the input signal.

7. The reset circuit according to claim 6,
wherein among the plurality of delay means, delay means
arranged at a last stage outputs the delayed reset signal
5 to the control means.

8. A reset circuit which includes a plurality of
asynchronous modules and a plurality of synchronous modules
from a first state to a last stage for executing desired
10 functions, and initializes each of the pluralities of
asynchronous and synchronous modules arranged in a
semiconductor integrated circuit, comprising:

input means for inputting a reset signal to
initialize the plurality of asynchronous modules; and

15 pulse generation means connected to the input
means to generate a reset pulse based on the reset signal,
wherein:

the plurality of asynchronous modules include a
first asynchronous module arranged at a first stage, which
20 is connected to an output of the pulse generation means and
receives the reset pulse to be initialized, and a second
asynchronous module arranged at a next stage;

the first asynchronous module has first control
means for generating a first reset signal to initialize the
25 second asynchronous module, and outputting the first reset
signal to the second asynchronous module after
initialization in the first asynchronous module; and

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the second asynchronous module has second control means which is connected to an output of the first asynchronous module, receives the first reset signal output from the first asynchronous module to be initialized, generates a second reset signal to initialize an asynchronous module arranged at a further next stage based on the first reset signal from the first asynchronous module, and outputs the second reset signal after initialization in the second asynchronous module, the reset circuit further comprising:

clock input means for inputting a clock signal;

third control means connected to the second asynchronous module to output, upon detection of the second reset signal, a control signal corresponding to the second reset signal for a period until a last delayed reset signal is input for a synchronous module of a last stage; and

a plurality of delay means connected to the clock input means to delay an input signal in synchronization with the clock signal, and to output a delayed reset signal generated by the delaying, wherein:

the plurality of synchronous modules are connected corresponding to the plurality of delay means, operated in synchronization with the clock signal, and initialized in synchronization with the clock signal based on the control signal and the delayed reset signal; and

among the plurality of delay means, first delay means arranged at a first stage receives the control signal

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output from the third control means as the input signal,
and each of second delay means arranged at stages
thereafter receives the delayed reset signal output from
delay means arranged at a previous stage as the input
5 signal.